## **Register Map**

Segment Address	0	1	2	3	4	5
00~0F	Status Register	Input			Memory	ADC
10~1F	(Read Only)	Formatter	De-interlace		Chapter 05	Chapter 11
20~2F	Chapter 00	Chapter 01	Chapter 02	Video	Capture &	
30~3F		UD bypace		Processor	Playback, Chapter 06	Sync Proc
40~4F	Miscellaneous	HD-bypass Chapter 03		Chapter 08	Read FIFO, Write FIFO	Chapter 12
50~5F	Chapter 04	Chapter 00			Chapter 07	Chapter 12
60~6F		Mode Detect				
70~7F		Chapter 10		PIP Chapter 08		
80~8F		Chapter 10				
90~9F	OSD Chapter 09					
A0~AF						
B0~BF						
C0~CF						
D0~DF						
E0~EF						

## Note:

- 1. Address marked with is not existed in 5725.
- 2. All registers (except **chapter 01** status register is read only) have default value "0x00" after power up.
- 3. All registers require segment for access. Segment is defined in address F0. For example:
  - S1\_46 means F0 must be set to 1 before accessing 46
  - S1\_46=8D equal following operation:

F0 = 01

46 = 8D